CLAIMS:

1. Data processing system comprising:

- a clustered Instruction Level Parallelism processor, comprising a plurality of clusters (A – D) each comprising at least one register file and at least one functional unit;

- an instruction unit (IFD) for issuing control signals to said clusters (A – D), wherein said instruction unit (IFD) is connected to each of said clusters (A – D) via respective control connections (CA – CD), and

wherein one or more additional pipeline register (P) is arranged in said control connections (CA – CD) depending on the distance between said instruction unit (IFD) and said clusters (A – D).

2. Data processing system according to claim 1, wherein

said clusters (A – D) are connected to each other via a point-to-point connection.

3. Data processing system according to claim 1, wherein

said clusters (A – D) are connected to each other via a bus connection (100).

4. Data processing system according to claim 3, wherein

said control connections (CA – CD) are implemented as a bus (110).

5. A clustered Instruction Level Parallelism processor, comprising:

- a plurality of clusters (A – D) each comprising at least one register file and at least one functional unit;

- an instruction unit (IFD) for issuing control signals to said clusters (A – D), wherein said instruction unit (IFD) is connected to each of said clusters (A – D) via respective control connections (CA – CD), and

wherein one or more additional additional pipeline register (P) is arranged in said control connections (CA – CD) depending on the distance between said instruction unit (IFD) and clusters (A – D).